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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/932,330	08/17/2001	Jon M. Huppenthal	SRC012	4801

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EXAMINER
SORRELL, ERON J

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/932,330	HUPPENTHAL ET AL.	
	Examiner	Art Unit	
	Eron J. Sorrell	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
AU2181

Supervisory 4/4/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-4,7-10,12-16, and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster (U.S. Patent No. 6,052,134) in view of O'Sullivan (U.S. Patent No. 4,972,457).

3. Referring to claim 1, Foster teaches a computer system (see figure 1) comprising:

at least one processor (see item 12 of figure 1);

a controller (see item 14 in figure 2) for coupling the at least one processor to a peripheral bus control block (see item 28 in figure 1 and a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one peripheral bus slot coupled to the peripheral bus control block by a peripheral bus (see item 30a in figure 1 and lines 14-25 of column 6)

at least one memory module slot coupled to the memory module bus (see lines 30-55 of column 5).

Foster fails to teach the system further comprises a processor element associated with the at least one memory module slot for providing a direct data connection to an external device connected thereto and the memory module slot enabling data exchange directly between the external device and the memory module bus.

O'Sullivan teaches a computer system comprising the above limitations (see item 70 in figure 4 and lines 50-59 of column 5 and lines 7-41 of column 7), and suggests the processor element (hybrid communications control unit), can be located in any available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

4. Referring to claim 13, Foster teaches a computer system (see figure 1) comprising:

at least one processor (see item 12 of figure 1);

a controller (see item 14 in figure 2) for coupling the at least one processor to a graphic bus control block (see item 20 in figure 1 and a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one graphics bus connection coupled to the graphics bus control block by a peripheral bus (see item 24 in figure 1 and paragraph bridging columns 5 and 6)

at least one memory module slot coupled to the memory module bus (see lines 30-55 of column 5).

Foster fails to teach the system further comprises a processor element associated with the at least one memory module slot for providing a data connection to an external device connected thereto.

O'Sullivan teaches a computer system comprising the above limitations (see item 70 in figure 4 and lines 50-59 of column 5 and lines 7-41 of column 7), and suggests the processor element (hybrid communications control unit), can be located in any available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the

system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

5. Referring to claims 2 and 14, O'Sullivan teaches a control connection to the peripheral port (see bus coupling item 70 to item 78 in figure 4) for indicating to the at least one processor an arrival of data on the direct data connection to the processor element and the memory module slot (see lines 1-18 of column 6).

6. Referring to claims 3 and 15, Foster teaches memory module bus comprises a DIMM bus (see paragraph bridging columns 6 and 7; Note DIMMs have a 64-bit width and Foster discloses the memory banks disclosed have a 64-bit width).

7. Referring to claims 4 and 16, O'Sullivan teaches the processor element comprises a DIMM physical format for retention within one of the DIMM memory module slots.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

8. Referring to claims 7 and 19, O'Sullivan teaches the external device comprises one of another computer system, switch or network (see item 40 in figure 4).

9. Referring to claim 8, Foster teaches the peripheral bus comprises a PCI bus (see item labeled PCI bus in figure 1).

10. Referring to claims 9,10,21, and 22 O'Sullivan teaches the processor element is operative data received from said controller on said memory bus and is operative alter data received from an external source prior to placing altered data said memory bus (see lines 3-12 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the

system of Foster with the above teachings of O'Sullivan in order for the data to be in the proper format/protocol for sending and receiving data.

11. Referring to claims 12 and 23, Foster the at least one processor comprises a plurality of processors (see lines 13-36 of column 1).

12. Referring to claim 20 and 24, Foster teaches the graphics bus comprises an AGP bus (see bus connecting items 14 and 20 in figure 1).

13. Claims 5,6,17,18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claims 1 and 34 above, and further in view of Tetrick (U.S. patent No. 6,598,199).

14. Referring to claims 5,6,17,18 the combination of Foster and O'Sullivan fails to teach the memory module slots comprise inline serial memory module slots and the adapter port comprises a inline serial memory module physical format for retention within one of said inline serial memory module slots.

Tetrick teaches the inline memory module substantially similar to DIMMs, but use RDRAM chips which have faster access times than other DRAM or SDRAM chips (see lines 40-54 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the above teachings of Tetrick in order to use a faster memory as suggested by Tetrick.

15. Claims 11 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claims 1 and 13 above, and further in view of Chiles et al. (U.S. Patent No. 6,581,157).

16. Referring to claims 11 and 23 the combination of Foster and O'Sullivan fails to teach the processor element further comprises at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said processor element.

Chiles teaches the above limitation (see item labeled 256 in figure 3 and paragraph bridging columns 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the

combination of Foster and O'Sullivan with the teachings of Chiles. One of ordinary skill would have been motivated to make such modification in order to upgrade the adapter port without purchasing a new one.

17. Claims 25-28,31-34 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan and further in view of Whittaker et al. (U.S. Patent No. 5,889,959 hereinafter "Whittaker").

18. Referring to claim 25, Foster teaches a computer system (see figure 1) comprising:

at least one processor (see item 12 of figure 1);

a controller (see item 14 in figure 2) for coupling the at least one processor to a memory bus (see bus coupling item 14 to item 18 in figure 1);

at least one memory module slot coupled to the memory module bus (see lines 30-55 of column 5).

Foster fails to teach the system further comprises a controller for coupling the processor with a maintenance control block and a processor element associated with the at least one memory module slot for providing a direct data connection to an external device connected thereto and the memory module slot

enabling a data exchange directly between the external device and the memory module bus.

O'Sullivan teaches a computer system comprising and a processor element associated with the at least one memory module slot for providing a direct data connection to an external device connected thereto and the memory module slot enabling a data exchange directly between the external device and the memory module bus (see item 70 in figure 4 and lines 50-59 of column 5 and lines 7-41 of column 7), and suggests the processor element (hybrid communications control unit), can be located in any available memory expansion slot within the computer.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

The combination of Foster and O'Sullivan fails to teach the control block comprises systems maintenance control block, wherein the systems maintenance control block provides control information to the processor element.

Whittaker teaches a control block comprising a systems maintenance control block, wherein the systems maintenance control block provides control information processor element (see lines 42-49 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the above teachings of Whittaker. One of ordinary skill in the art would have been motivated to make such modification in order to provide diagnostic functions to all of the modules in the system as suggested by Whittaker (see lines 30-43 of column 1).

19. Referring to claim 26, O'Sullivan teaches a control connection to the peripheral port (see bus coupling item 70 to item 78 in figure 4) for indicating to the at least one processor an arrival of data on the data connection to the processor element (see lines 1-18 of column 6).

20. Referring to claim 27, Foster teaches memory module bus comprises a DIMM bus (see paragraph bridging columns 6 and 7; Note DIMMs have a 64-bit width and Foster discloses the memory banks disclosed have a 64-bit width).

21. Referring to claims 28, O'Sullivan teaches the processor element comprises a DIMM physical format for retention within one of the DIMM memory module slots.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan. One of ordinary skill in the art would have been motivated to make such modification in order to add an adapter using an existing available slot without making any hardware changes in the computer or purchasing additional equipment as suggested by O'Sullivan.

22. Referring to claims 31, O'Sullivan teaches the external device comprises one of another computer system, switch or network (see item 40 in figure 4).

23. Referring to claim 32, Whittaker teaches the system maintenance bus comprises a SM bus (see item 12B in figure 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan for the same reasons as outlined in the rejection of claim 25, supra.

24. Referring to claims 33 and 34 O'Sullivan teaches the processor element is operative data received from said controller on said memory bus and is operative alter data received from an external source prior to placing altered data said memory bus (see lines 3-12 of column 4).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Foster with the above teachings of O'Sullivan in order for the data to be in the proper format/protocol for sending and receiving data.

25. Referring to claims 36, Foster the at least one processor comprises a plurality of processors (see lines 13-36 of column 1).

26. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan as applied to claims 25 above, and further in view of Tetrick (U.S. Patent No. 6,598,199).

27. Referring to claims 29 and 30 the combination of Foster and O'Sullivan fails to teach the memory module slots comprise inline serial memory module slots and the adapter port comprises

a inline serial memory module physical format for retention within one of said inline serial memory module slots.

Tetrick teaches the inline memory module substantially similar to DIMMs, but use RDRAM chips which have faster access times than other DRAM or SDRAM chips (see lines 40-54 of column 2).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the above teachings of Tetrick in order to use a faster memory as suggested by Tetrick.

28. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Foster in view of O'Sullivan and further in view of Whittaker as applied to claim 25 above, and further in view of Chiles et al. (U.S. Patent No. 6,581,157).

29. Referring to claims 36 the combination of Foster, O'Sullivan, and Whittaker fails to teach the processor element further comprises at least one field programmable gate array configurable to perform an identified algorithm on and operand provided thereto by said processor element.

Chiles teaches the above limitation (see item labeled 256 in figure 3 and paragraph bridging columns 8 and 9).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Foster and O'Sullivan with the teachings of Chiles. One of ordinary skill would have been motivated to make such modification in order to upgrade the adapter port without purchasing a new one.

Response to Arguments

30. The outstanding Double Patenting rejection is hereby withdrawn. While there are similarities between the claimed structural elements of the instant application and application 10/869,199, the claims are patentably distinct because the claims of the instant application as amended, are directed toward communications between an external device and a memory bus, by way of a processor element associated with a memory module slot coupled to the memory bus, whereas the claims of applications 10/869,199 are directed toward controlling memory accesses from an internal dense logic device to memory resources located on an adapter port associated with a memory module slot.

31. Applicant's arguments filed 1/11/06 regarding the outstanding prior art rejections have been fully considered but they are not persuasive. The applicant argues:

1) O'Sullivan fails to teach a processor element associated with at least one memory module slot for providing a direct data connection between an external device coupled thereto and the memory module bus (see 2nd and 3rd paragraph of page 10).

2) O'Sullivan states that "Since the hybrid communications protocol unit 68 may be installed in the computer 90, it should be recognized that, for so me [sic] applications, the microprocessor 70 can be performed by the computer 90", thus the processing performed by the applicant's invention that allows and manages a direct exchange of data between an external device and the memory module bus cannot be accomplished by the computer (see second paragraph on page 11).

3) The long felt need to provide an interface between main memory and an external device and lack of such interface prior to the applicant's invention is also evidence that one skilled in the art would not look to O'Sullivan, issued in 1990, to couple external devices directly to a memory bus (see first full paragraph on page 12).

32. As per argument 1, the Examiner disagrees. O'Sullivan clearly teaches the hybrid communications card can be coupled to a memory module slot. At lines 30-37 of column 7, O'Sullivan teaches "In addition, the card of hybrid communications control

unit 68 could be installed ***in a many locations*** other than modem slot 89 (emphasis added). For example the card could be installed ***in a memory expansion or other expansion slot*** of computer." Clearly from this citation, one of ordinary skill in the art would recognize the memory expansion slot to be a slot for holding additional memory modules, especially since it is distinguished from "other expansion slots." In the example illustrated by O'Sullivan, when the hybrid communication card is installed in a memory expansion slot, the external devices would be in direct communication with the memory bus of the computer. A Terminal Disclaimer is no longer required.

33. As per argument 2, the Examiner disagrees. The citation from O'Sullivan shows that the functions of the microprocessor and be performed by the computer, in some applications, however, it's clear from the citation that this is not the case in all applications. Furthermore, the details of the operation of the processor element are not claimed by the applicant. The claims only require the processor element provide a direct data connection to the memory bus an enable data exchange direct between the external device and the memory module bus. The processor element of O'Sullivan provides that functionality as evidenced in figure 4. Figure 4 shows communications from

external devices passing through the microprocessor to the interface then on to the computer.

34. As per argument 3, the Examiner disagrees. Per MPEP 2145, "The mere age of the references is not persuasive of the unobviousness of the combination of their teachings, absent evidence that, notwithstanding knowledge of the references, the art tried and failed to solve the problem." In re Wright, 569 F.2d 1124, 1127, 193 USPQ 332, 335 (CCPA 1977) (100 year old patent was properly relied upon in a rejection based on a combination of references.). See also Ex parte Meyer, 6 USPQ2d 1966 (Bd. Pat. App. & Inter. 1988) (length of time between the issuance of prior art patents relied upon (1920 and 1976) was not persuasive of unobviousness).

Conclusion

35. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened

statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J. Sorrell whose telephone number is 571 272-4160. The examiner can normally be reached on Monday-Friday 8:00AM - 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EJS
April 11, 2006

Supervisory

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100
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4/14/2006